Fabrication of Si tunnel diodes for III-V / Si tandem solar cells

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Increasing competitiveness of photovoltaic (PV) devices is currently an important objective in technological research and since fabrication costs of PV modules now tend to stabilize, improvement is achievable only by increasing module efficiency. Therefore, efforts have been made to develop tandem solar cells (i.e. cells obtained by coupling two different units, a top and a bottom one) based on III-V/Si layers.

The role of the tunnel-junction in such tandem cell is to offer a low resistance connection between the top (III-V) and bottom cell (Si). In our approach, the tunnel junction is realised within the bottom Si cell with degenerated layers n++ / p ++ very thin layers. Several processes can be used for the fabrication of tunnel diodes, among them, spin-on doping (SOD) combined with a rapid thermal annealing (RTA) was chosen. Precursor solutions are Phosphorofilm and Borofilm and are deposited on a supporting Si wafer (called “source wafer”), then dried 10 min at 200°C in order to remove solvents and to form the oxide (B or P dispersed in SiO2 matrix).

In order to carefully control diffusion of boron and phosphorus into the target wafer, a technique called proximity rapid thermal processing was developed, and involves placing the source wafer in proximity to the device wafer with a short distance in between. Annealing temperature range is 900-1000°C during few seconds under N_2 atmosphere.

In this communication we will present our experimental results regarding fabrication of Si tunnel diodes on (100) Si wafers. We fabricated p++/n++ and n++/p++ devices that are characterized using Electrochemical Capacitance Voltage Profiling (ECV) in order to determine doping and depth of each layers. Later, I(V) are presented to evaluate the quality of the tunneling effect.

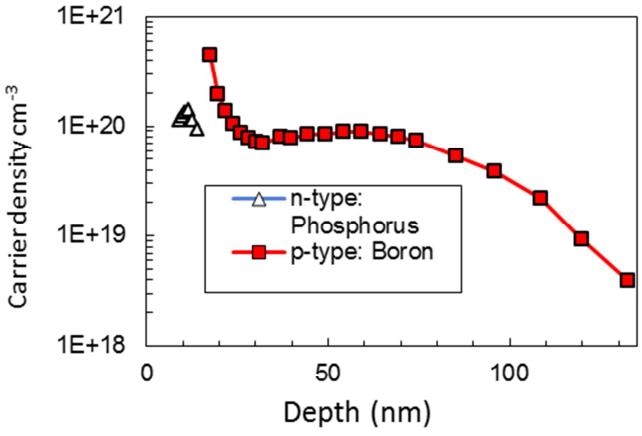

Fig 1: ECV doping profile of a n++/p++ structure

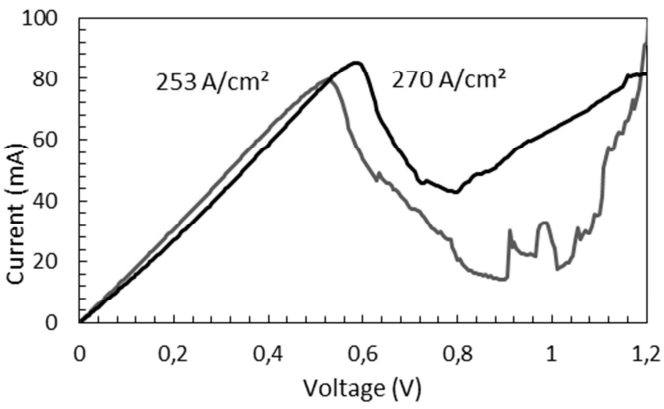

Fig 2: I(V) characteristic of n++/p++ tunnel diode on p+ substrate